REMARKS

The Office Action dated January 12, 2004 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Claims 1-22 are pending in the instant application and have been examined. Claims 2-9, 11, 12, 15, 16, 18 and 22 were objected to as being dependent on rejected base claims, but indicated as being allowable if rewritten in independent form. Claims 1-22 are again submitted for consideration.

Claim 1 was rejected under 35 U.S.C. 103(a) as being unpatentable over *Takahashi* (U.S. Patent No. 5,239,381) in view of *Miller et al.* (U.S. Patent No. 6,275,546). Claims 10, 13, 14, 17 and 19-21 were rejected under 35 U.S.C. 103(a) as being unpatentable over *Miller et al.* in view of *Takahashi*. The above rejections are respectfully traversed according to the remarks that follow.

The present invention is directed, according to claim 1, to a method for storing data. The method includes generating a glitchless fractional clock pulse in a circuit, transmitting the glitchless fractional clock pulse from the circuit to a data storage element and storing data in the storage element upon receiving the glitchless fractional clock pulse.

The present invention is also directed, according to claim 10, to a method for enabling a latch. The method includes receiving a clock signal in a logic circuit, receiving a latch enable pulse in the logic circuit, generating a glitchless fractional clock pulse in the logic circuit in response to the latch enable pulse and the clock signal and

transmitting the glitchless fractional clock pulse to a gate input of a latch to enable the latch to store data during an optimally stable time period.

The present invention is directed, according to claim 13, to an apparatus for storing data. The apparatus includes at least one storage element having a data input, a storage enable input, and a data output and at least one logic circuit having an activating input, an clock input, and a logic output. The at least one logic circuit generates a glitchless fractional clock pulse on the logic output, the logic output is connected to the storage enable input of the storage element and operates to enable the at least one storage element to store data resident on the data input at an optimally stable time.

The present invention is directed, according to claim 17, to a network switch for switching data. The network switch includes at least one data port interface, at least one storage element in connection with the at least one data port interface and having a data input, a storage enable input, and a data output and at least one logic circuit having an activating input, a clock input, and a logic output. The at least one logic circuit is configured to generate a glitchless fractional clock pulse on the logic output, the logic output being connected to the storage enable input of the storage element and operating to enable the at least one storage element to store data resident on the data input at an optimally stable time.

The present invention is directed, according to claim 20, to an apparatus for storing data. The apparatus includes a storage means for storing data, the storage means having an input for receiving data to be stored, a storage enable input for enabling the

storage means, and a data output and at least one pulse generating means for generating a glitchless fractional clock pulse, the pulse generating means having an activating input, a clock input, and an output in connection with the storage enable input of the storage means. The pulse generating means generates the glitchless fractional clock pulse that is transmitted to the storage means to enable the storage means to store data at an optimally stable time.

Takahashi is directed to an apparatus for recording and reproducing a plurality of television signals of different systems. The Office Action appears to rely on this reference for its alleged teaching of a buffer memory and means for controlling the buffer memory, where the buffer controller selects a period in response to a write clock signal. The Office Action acknowledges that *Takahashi* fails to disclose that the write clock signal is a glitchless fractional clock pulse and thus also cites *Miller et al.*

Miller et al. is directed to a glitchless clock switch circuit, for producing an output clock signal that is selectively synchronized to one of two generally free-running input clock signals. The Office Action appears to acknowledge that *Miller et al.* does not disclose a "glitchless fractional clock pulse," but rather alleges that "[t]he specification does not provide a definition for "factional," so any glitchless clock pulse is a glitchless fractional clock pulse." However, Applicants respectfully traverse the latter finding and, additionally, the rejections, as discussed below.

Contrary to the position adopted in the Office Action, Applicants respectfully assert that the instant specification does provide a definition for "fractional," as used in

"glitchless fractional clock pulse," in independent claims 1, 10, 13, 17 and 20. A definition of "fractional" may be found in the instant specification at page 62, line 28 to page 63, line 11:

> PMMU 70 further utilizes novel structure and logic within the respective FIFO's to optimally store data within storage units. This structure and logic generally includes generating a glitchless fractional clock pulse from an increment or enable pulse and a clock signal, which is provided to a storage element to enable a data storage operation in a time period in which the data to be stored is most stable. The glitchless fractional clock pulse, which is generally of a shorter period than the system core clock pulse and asserted high during the same time period or duration that the core clock pulse is asserted high, defines a region in which the data to be stored is in an predicably stable state. The predictably stable state is a result of the data being stable in the median region of the clock pulse, as opposed to the end regions proximate the rising and falling edge of the clock pulse, where the data tends to be unstable. The structure and logic of the present invention not only allows for storage of data during a predictably stable portion of a clock cycle, but also minimizes overhead consumption via usage of simple space saving elements.

In addition, a glitchless fractional clock pulse is illustrated in Fig. 32, in the waveform indicated as being "Gate[i]." As such, Applicants respectfully assert that the present specification and claims clearly define the fractional aspect of the glitchless

fractional clock pulse, so that the indication in the rejections of the claims, that any glitchless clock pulse is a glitchless fractional clock pulse, is incorrect and should be withdrawn. Additionally, neither cited reference, *Takahashi* nor *Miller et al.*, teaches or suggests such a glitchless fractional clock pulse. Thus, Applicants respectfully assert that the rejections of claims 1, 10, 13, 14, 17 and 19-21 are improper because the rejections fail to teach or suggest all of the elements of those claims. Reconsideration and withdrawal of the rejection are respectfully requested.

In addition, Applicants also note that claim 17 is directed to a network switch for switching data. The specification clearly discusses the elements and functioning of a network switch. Applicants note that neither cited reference, *Takahashi* nor *Miller et al.*, teaches or suggests a network switch for switching data. Thus, for this additional reason, Applicants respectfully assert that the rejection of claims 17-19 is improper and should be withdrawn.

Similarly, Applicants respectfully assert that claims 2-9, 11, 12, 14-16, 18, 19, 21 and 22 should be allowed for at least their dependence on independent claims 1, 10, 13, 17 and 20, although Applicants acknowledge that most of those claims have already been indicated as containing allowable subject matter. Thus, Applicants respectfully assert that all rejections of the claims should be withdrawn and that application should be allowed to proceed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by

telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

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Enclosures: Formal Drawings
Copy of Notification of Change of Name and Address and Associate Power of Attorney filed April 8, 2004